

WE CLAIM:

1 1. A method for generating computer system level architectures that are
2 capable of executing multiple functional specifications, given a set of physical resources,
3 and subject to a set of design constraints, the method comprising:

4 forming an initial master task graph from said multiple specifications, said
5 initial master task graph including at least one hierarchical task having pointers to a
6 plurality of sub-task graphs, and at least one attribute selected from a group comprising
7 an AND attribute and an XOR attribute;

8 processing said initial master task graph to provide a selected number of
9 final master task graphs, each of said final master task graphs comprising a list of AND
10 task graphs;

11 generating a family of architectures for each of said final master task
12 graphs, each of the architectures generated for a given final master task graph being
13 capable of executing every AND task graph included in the list for the given final master
14 task graph; and

15 exploring each of said generated architectures for use in executing said
16 multiple specifications.

1 2. The method of Claim 1 wherein:

2 said initial master task graph includes a first hierarchical task having an
3 AND attribute, and a second hierarchical task having an XOR attribute.

1 3. The method of Claim 2 wherein said processing step comprises:
2 resolving said initial master task graph into sets of AND task graphs on
3 the basis of respective sub-task graphs associated with said first hierarchical task; and
4 resolving said sets of AND task graphs into said final master task graphs.

1 4. The method of Claim 1 wherein:
2 said given final master task graph is applied to an architecture synthesis
3 engine to generate a family of architectures therefor.

1 5. The method of Claim 1 wherein said exploring step comprises:
2 placing each of the architectures generated for said given final master task
3 graph into a pool; and
4 retaining a particular architecture in said pool only if said particular
5 architecture can execute each AND task graph of said given final master task graph in
6 accordance with a prespecified time schedule.

1 6. The method of Claim 1 wherein:
2 a generated architecture is disposed to execute specified multiple tasks
3 from said task specifications on a single component that is selected from said set of
4 resources.

1 7. The method of Claim 1 wherein:

2 a generated architecture is disposed to execute specified multiple tasks
3 from said task specifications on the same type, but different instances, of a component
4 that is selected from said set of resources.

1 8. An article of manufacture for generating system level architectures that
2 are capable of executing multiple functional specifications, given a set of physical
3 resources, and subject to a set of design constraints, said article of manufacture
4 comprising:

5 a computer readable medium;
6 a plurality of instructions wherein at least a portion of said plurality of
7 instructions are storable in said computer readable medium, and further wherein said
8 plurality of instructions are configured to cause a processor to:
9 form an initial master task graph from said multiple specifications,
10 said initial master task graph including at least one hierarchical task having pointers to
11 a plurality of sub-task graphs, and at least one attribute selected from a group comprising
12 an AND attribute and an XOR attribute;
13 process said initial master task graph to provide a selected number
14 of final master task graphs, each of said final master task graphs comprising a list of
15 AND task graphs;
16 generate a family of architectures for each of said final master task
17 graphs, each of the architectures generated for a given final master task graph being
18 capable of executing every AND task graph included in the list for the given final master
19 task graph; and

20 explore each of said generated architectures for use in executing
21 said multiple specifications.

1 9. The article of manufacture of Claim 8 wherein:
2 said initial master task graph includes a first hierarchical task having an
3 AND attribute, and a second hierarchical task having an XOR attribute.

1 10. The article of manufacture of Claim 9 wherein said processing step
2 comprises:
3 resolving said initial master task graph into sets of AND task graphs on
4 the basis of respective sub-task graphs associated with said first hierarchical task; and
5 resolving said sets of AND task graphs into said final master task graphs.

1 11. The article of manufacture of Claim 8 wherein:
2 said given final master task graph is applied to an architecture synthesis
3 engine to generate a family of architectures therefor.

1 12. The article of manufacture of Claim 8 wherein said exploring step
2 comprises:
3 placing each of the architectures generated for said given final master task
4 graph into a pool; and
5 retaining a particular architecture in said pool only if said particular
6 architecture can execute each AND task graph of said given final master task graph in
7 accordance with a prespecified time schedule.

1 13. The article of manufacture of Claim 8 wherein:
2 a generated architecture is disposed to execute specified multiple tasks
3 from said task specifications on a single component that is selected from said set of
4 resources.

1 14. The article of manufacture of Claim 8 wherein:
2 a generated architecture is disposed to execute specified multiple tasks
3 from said task specifications on the same type, but different instances, of a component
4 that is selected from said set of resources.

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